ASYNCHRONOUS, INDEPENDENT AND MULTIPLE
PROCESS SHARED MEMORY SYSTEM
5
IN AN ADAPTIVE COMPUTING ARCHITECTURE

Abstract of the Disclosure

The present invention provides a system and method for implementation and use of a shared memory. The shared memory may be accessed both independently

10   and asynchronously by one or more processes at corresponding nodes, allowing data to be streamed to multiple processes and nodes without regard to synchronization of the plurality of processes. The various nodes may be adaptive computing nodes, kernel or controller nodes, or one or more host processor nodes. The present invention maintains memory integrity, not allowing memory overruns, underruns, or deadlocks. The present

15   invention also provides for "push back" after a memory read, for applications in which it is desirable to "unread" some elements previously read from the memory.